Substrate Condition and Metrology Considerations in Poly Gate Doping Implants

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***Abstract*— The evolution from planar to 3D structures in advanced memory devices has resulted in semiconductor equipment manufacturers facing unprecedented challenges in delivering products that can demonstrate simultaneous compliance to the productivity, reliability and process requirements of their customers. In the field of ion implantation, these challenges are driven by: (i) the increasing prevalence of hard mask and removal of PR stripping process and (ii) the transition from the use of implants in dopant application to that of materials modification. These have resulted in large reductions in both the particle size and number density that can be tolerated from implant steps.**

One area where these issues have proven challenging is that of contact engineering. Low energy phosphorus implants are used to improve the contact resistivity of poly Si contact. This is critical for the read/write time of the storage node capacitor in DRAM operation. As devices shrink further, the thickness of the poly gate in the peripheral transistors become as low as a few hundred Å. This results in a phosphorus implant requirement of ~1keV. Depletion in the poly Si gate requires a few keV implant energy for poly doping for both NMOS and PMOS. In order to maintain proper gate operation, gate doping requires around E15 doses. This places a large amount of implanted phosphorus at or near the surface of the wafer.

In this paper, a phenomenon is described where the magnitude of surface particles arising from phosphorus implants is a function of the reaction between implanted phosphorus and ambient atmosphere. Using SEM/EDX, spatial

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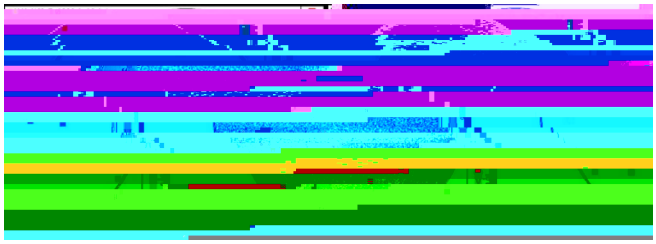

Fig. 1. Effect of delay on measured particle map

For DRAM devices, low energy high dose implantation historically has been applied across the transistor structure with different goals. For shallow junction formation these include precise dose control, across wafer uniformity (afforded by beam angle control), optimization of co-implant and damage engineering. For materials modification implants such as contact implant to Si and/or poly-Si, cross contamination, energy contamination and optimization of dose rate control have been required to meet device node requirements. Defect control including understanding particle generation, monitoring and control as well as productivity improvements are strongly linked to device requirements and are a key component of hardware/software development in implanter technology.

Modern high current ion implanters, such as the Axcelis Purion H2™, provide enhanced productivity for the hig1sb(h)9ePsor sst i bplentst122ar Tw Td [((af)11e dos(cu)9(reng(Modern

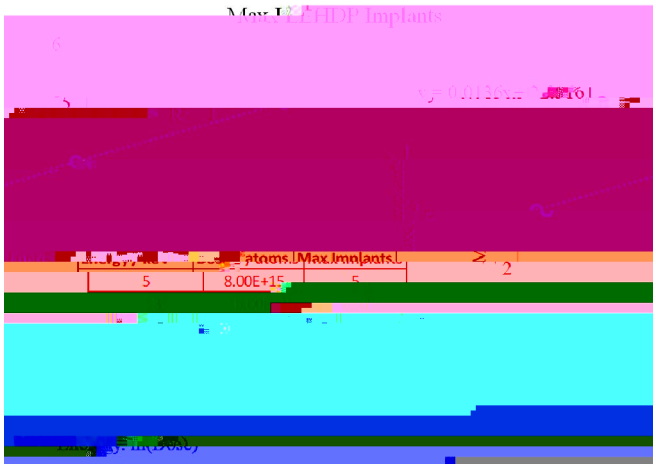

Fig. 2. Max implants as a function of energy and dose

The proposed mechanism for this observed issue is the large amount of surface Phosphorus resulting from the implant. Typical LEHDP SIMS profiles are shown in Fig. 3 (the three traces represent different tool configurations). As the implant energy reduces, and/or the dose increases, the magnitude of this surface concentration will rise. Further factors known to occur which could conflate this process are the segregation of Phosphorus at the Si-SiO_2 interface and migration of the implanted Phosphorus back to the surface.

Secondly, let us consider the time dependence. Initial observations of the phenomenon had occurred when wafers that had been implanted, post measured showing very low adder counts, and then re-measured the next morning, showed >1e3 particles on the surface. These wafers had been left in a non-purged but sealed FOUP at ambient in the class ten clean room. It was found that by double bagging and sealing the wafers the probability of elevated particle on re-measurement could be reduced but not eliminated. Even at ~ 2hours at 40% RH there was sufficient reaction with ambient air to result in large counts on remeasurement. Below 1 hour no elevation was observed. This has led us to conclude that a maximum measurement delay of 90mins from implant is advisable for LEHDP implants, however as this study did not determine the impact of exposure to different RH levels this may be a function of RH. Typical spec for semiconductor manufacturing equipment is an RH of 40-45%, balancing avoiding both electrostatic discharge and condensation on cooled surfaces. Many Fabs typically operate at or below the lower end of this range – measurement on weather stations attached to many tools read 36-40% RH. With the increasing prevalence of N_2-purged FOUPs it is likely that this time to measurement can be extended, and this is proposed for further study.

Analysis of the particles themselves yielded the following information: From the SurfScan™ data, defects arising on the wafer from small numbers of implants are random in location and are in general < 15 adders / pass at > 32nm. The lack of characteristic spatial patterns indicate that they do not arise from a mechanical source or a high voltage discharge event such as an insulator breakdown or arcing between graphite electrodes. It is postulated that the majority of particles in LEHDP operation arise from beam clipping on graphite apertures in the near wafer environment. Since the incident ion energy is very low, the likely particle source is not the graphite itself but beam interactions with deposited material on these apertures.

Fig. 3. Typical LEHDP SIMS profiles (three h/w configurations shown)

The particle size distribution indicates that this phenomenon may have been occurring for some time in production. It is only with the transition to smaller particle sizes in offline metrology (minimum bin size at 45nm or below) does the issue become noticeable. Due to the large